

2nd H17  
33. (New) A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region; and

a trench capacitor formed in a trench and coupled to the first source/drain region;

wherein the trench capacitor includes a polysilicon plate formed in the trench that is coupled to the first source/drain region, a second plate formed by the substrate with a surface of the substrate in the trench roughened by etching a polysilicon material on the surface of the substrate with an etching process selected from the group consisting of an anodic etch and a phosphoric acid etch, and an insulator layer that separates the polysilicon plate from the roughened surface of the substrate

Sub. C3  
B1  
34. (New) A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface; and

a trench capacitor with a plate that is formed in a trench that surrounds a roughened surface of the first source/drain region of the transistor;

wherein the roughened surface of the first source/drain region of the transistor is formed by etching the layer of polysilicon using an etch process selected from the group consisting of an anodic etch and a phosphoric acid etch.

35. (New) A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor includes a micro-roughened surface of porous polysilicon and a second plate of the trench capacitor is disposed adjacent to the first plate, wherein the micro-roughened surface of porous polysilicon is formed by etching a layer of polysilicon using an etch process selected from the group consisting of an anodic etch and a phosphoric acid etch;

**SUPPLEMENTAL PRELIMINARY AMENDMENT**

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Title: CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES (as amended)

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Sub. C3 cond.  
B1  
a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

Concl'd Sub F10  
36. (New) The memory device of claim 35, wherein the access transistor comprises a lateral transistor that is coupled to the second plate of the trench capacitor.

**REMARKS**

*Title*

Applicant has amended the Title for consistency with the pending claims.

*New Claims*

Applicant respectfully submits that new claims 31-36 comport with the definition of the elected species as Applicant understands the definition provided by Examiner Olik Chaudhuri in Paper No. 7 of U.S. Patent Application Serial No. 09/010,729, the parent of this divisional application. Applicant thus requests entry and consideration of new claims 31-36.